REMARKS

Claims 2, 9, 10, 13, and 14 have been amended in view of the Section 112 rejections at pages 2-3 of the 04/13/2005 Office Action. Claim 19 has been cancelled and claims 20, 24, and 26 have been amended to depend from claim 1. New claims 33-41 have been added. New claims 33-36 and 40-41 are described at 0038 in the specification. The content of new claim 37 is described at 0012. The content of new claim 39 is described at 0034. Turning to the double-patenting rejections at pages 3-5 of the 04/13/2005 Office Action, a Terminal Disclaimer disclaiming over application serial no. 10/975,194 is enclosed. Application Serial No. 10/917,094 has claims to methods for removing a contaminant or film from a workpiece, or for removing an anti-reflective film. In contrast, the claims pending in the present application are directed to wafer thinning. As the objectives and end results between the two sets of claims are different, the pending claims are not obvious over the claims in Application Serial No. 10/917,094.

Regarding the Section 102(e) rejections at pages 6-7 of the 04/13/2005 Office Action, DeGendt *et al.*, USP 6,551,409, relates to methods for removing organic contaminants, such as photoresist, from a semiconductor surface. There is no suggestion in DeGendt *et al.*, of thinning a wafer. DeGendt *et al.* contemplates removing photoresist from a wafer, suggesting that devices have already been at least partially formed on the wafer. Consequently, DeGendt *et al.* clearly does not relate to wafer thinning, since wafer thinning would necessarily obliterate the devices on the wafer. In this sense, DeGendt *et al.* teaches away from wafer thinning.

The difference between removing an organic contaminant and thinning a wafer is significant. DeGendt *et al.* discusses removal of organic contaminants or photoresist

coatings that are 5 nm thick (column 6, line 28) or 4 nm (column 7, line 28). In one minute, 50% of the photoresist coating is removed (column 6, lines 33-38), using the immersion process shown in Fig. 3. In the moist vapor process shown in Fig. 2, photoresist is removed via 10 minutes of ozone processing followed by 10 minutes of rinse. Column 5, lines 47-56; column 6, lines 1-12. Accordingly, in DeGendt *et al.*, the photoresist etch rate is less than 5 nm/minute, and the material etched is an organic coating applied to the wafer, not the wafer itself.

In contrast, claims 1, 13, and 38 describe methods for thinning a silicon wafer. The chemical reactions involve the silicon material of the wafer itself, and not any organic coating on the wafer. Moreover, the end result is that the wafer itself is made thinner, i.e., silicon material is removed from the wafer, a concept unrelated to the content of DeGendt *et al.* The amount of material removed and the etch rates involved in wafer thinning are far higher than in DeGendt *et al.* DeGendt *et al.* therefore does not anticipate claims 1, 13, or 38.

In addition, claim 13 describes spraying DI water onto the wafer, and claim 38 describes applying an aqueous liquid onto the wafer, with the liquid forming a macroscopic liquid layer. DeGendt *et al.* does not suggest this step. The embodiment of DeGendt *et al.*, shown in Fig. 3 and described at column 6, lines 28-39 is an immersion process. Accordingly, the Fig. 3 embodiment of DeGendt *et al.* is entirely inconsistent with the spraying step of claim 13, or the formation of a macroscopic liquid layer step of claim 38.

The moist vapor method in DeGendt *et al.*, shown in Fig. 2 and described at column 5, lines 43 – column 6, line 14, results in a thin condensation layer formed on the wafer. Column 7, lines 4-6. However, no spraying as described in claim 13 is

involved, and no macroscopic liquid layer (formed by applying liquid – rather than via condensation) is disclosed or suggested by DeGendt *et al.* Claims 13 and 38 are therefore patentable over DeGendt *et al.* for these additional reasons.

Turning now to the rejections at pages 8-9 of the 04/13/2005 Office Action, EP 782177 relates to etching silicon oxide. Page 2, lines 12-15; page 3, lines 18-20; the Abstract; and claim 1. The silicon oxide is removed to provide a clean surface for subsequent processing. The oxide layers removed in EP 782177 are generally e.g., 1-2 nm thick. The wafer is e.g., 500,000 to 1,000,000 nm thick. Hence, removing a 1-2 nm oxide layer results in an insignificant change in thickness (of about .0002%). This is not wafer thinning. EP 782177 has no suggestion of wafer thinning, as claimed. To the contrary, the motivation in both EP 782177 and DeGendt *et al.* would be to remove only the organic or oxide layer, and leave all other layers, including the silicon itself entirely untouched. Accordingly, as neither DeGendt *et al.* or EP 782177 suggests any wafer thinning, the claims cannot be obvious over the combination of prior art applied at page 8 of the Office Action.

In addition, with respect to claims 30, 31, and 38, neither DeGendt *et al.* or EP 782177 suggest spinning the wafer to control the thickness of the aqueous liquid layer. In DeGendt *et al.*, the wafers are stationary. In EP 782177, spinning is performed to create a flow for rinsing, without regard to controlling a liquid layer thickness as claimed.

> "The etched wafer is spun and rinsed by conducting a stream of deionized liquid water onto the spinning wafer...."
> Page 2, lines 55-59.

> "The present invention includes an anhydrous HF gas and water vapor etch process, the etching process being completed by a rinsing step which includes conducting a stream of deionized liquid water onto a spinning wafer with anhydrous HF gas, HCL gas, ozone, or mixtures thereof being present...." Page 3, lines 22-26.

> "The rinse step may be controlled to meet the desired results by adjusting the rinse time, the spin rate, and/or the water flow rate." Page 3, lines 56-57.

Accordingly, in EP 782177, the spinning is performed to control the rinse step, without regard to the thickness of a liquid layer on the wafer, as claimed. Consequently, neither DeGendt *et al.*, or EP 782177, or the combination of them, disclose controlling a thickness of a liquid layer. Claims 30, 31, and 38 are patentable over the combination of DeGendt *et al.* and EP 782177, for this additional reason.

New claims 33, 34, and 41 describe wafer thinning methods having etch rates of more than 100 or 500 nm/minute. In contrast, in DeGendt *et al.*, 50% of a 5 nm thick photoresist coating is removed in one minute (column 6, lines 27-40) resulting in a removal rate of 2-3 nm/minute. Consequently, the etch rate of claim 33 is approximately 40 times faster, while the etch rate of claims 34 and 41 is approximately 200 times faster than in DeGendt *et al.* EP 782177 does not disclose any etch rates

whatsoever. Consequently, claims 33, 34, and 41 are patentable over the combination of DeGendt *et al.* and EP 782177, for this additional reason.

New claims 35, 37, and 40 describe reduction in wafer thickness. In DeGendt *et al.*, the photoresist coating removed is described as 5 nm (column 6, line 28), or 1.2 nm (column 6, line 62), or 4 nm (column 7, line 28). DeGendt *et al.* also describes a "thicker PR layer" of 1100 nm. One micron equals 1,000 nm. Accordingly, even using the 1100 nm PR layer thickness referenced in DeGendt *et al.*, claims 35, 36, and 40 describe a thinning process where the amount of material removed is hundreds of times greater than in DeGendt *et al.* EP 782177 has no disclosure on the amount of material removed. Accordingly, claims 35, 36, and 41 are patentable over the combination of DeGendt *et al.* and EP 782177, for this additional reason.

In view of the foregoing, it is submitted that the claims are in condition for allowance. A Notice of Allowance is requested.

Dated: July 8, 2005

Respectfully submitted,

PERKINS COIE LLP

Customer No. 45540
Perkins Coie LLP
Patent - LA
P.O. Box 1208
Seattle, WA 98111-1208
Phone: (310) 788-9900
Fax: (206) 332-7198

By: Kenneth H. Ohriner

Kenneth H. Ohriner
Reg. No. 31,646